What is claimed is:

[Claim 1] 1. A memory device, comprising:

a substrate, comprising a memory cell area and a peripheral circuit area, the memory cell area comprising a plurality of first trenches, the peripheral circuit area comprising a plurality of second trenches;

at least one stacked structure of memory cell disposed between two neighboring first trenches in the memory cell area over the substrate, the stack structure of memory cell comprising at least a tunneling layer, a floating gate, a inter-gate dielectric layer and a control gate;

a plurality of first isolation structures disposed between the neighboring stacked structures of memory cells in the memory cell area, the first isolation structure comprising:

a first liner disposed on sidewalls of the tunneling layer and the floating gate and a surface of the first trench; and

a first isolation layer covering the first liner, at least filling the first trenches;

at least one stacked device structure disposed between two neighboring second trenches in the peripheral circuit area over the substrate, the stacked device structure comprising at least a gate dielectric layer and a gate layer, wherein the gate dielectric layer covers part of the substrate; and

a plurality of second isolation structures disposed between neighboring stacked device structures in the peripheral circuit, the second isolation structure comprising:

a second liner disposed on a sidewall of the gate dielectric layer, a surface of the second trenches and a surface of the substrate not covered by the gate dielectric layer, the second liner having a round curve at an area not covered by the gate dielectric layer; and

a second isolation layer covering the second liner, at least filling the second trenches.

[Claim 2] 2. The memory device of claim 1, wherein the second liner layer at the area not covered by the gate dielectric layer is thicker than that in the other areas.

[Claim 3] 3. The memory device of claim 1, wherein the second trench is deeper than the first trench.

[Claim 4] 4. The memory device of claim 1, further comprising an additional floating gate disposed between the floating gate and the inter-gate dielectric layer.